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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,306	11/04/2003	Hea Suk Jung	CU-3424 VE	5038

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EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 09/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,306	JUNG, HEA SUK	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 14-15 are presented in the instant application.

RCE Response

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after advisory action. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 08/11/2006 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujieda et al. (U.S. Patent No. 6,181,174) in view of Muraki et al. (U.S. Patent No. 6,360,328).

With respect to claim 14, Fujieda et al. discloses, in Fig. 27, a synchronous memory device for synchronization of an external input clock [10] with an internal [output from 46A] input clock comprising a delay locked loop (DLL) having a clock divider [36,38], a power down controller [53] for determining a power down condition, and wherein the clock divider outputs a first clock signal and a second clock signal.

Fujieda fails to explicitly disclose that the clock divider outputs a first clock signal when the synchronous memory device is in a power down condition and a second clock signal when

the synchronous memory device is in a non-power down condition and wherein a frequency of the first clock signal is lower than that of the second clock signal.

Muraki et al. discloses, in column 1, lines 41 to 45, that one of various means for power down modes is to reduce the frequency of the clock and obviously clock divider is one of the means to reduce frequency of the clock.

It would have been obvious to one of ordinary skill in the art at the time of the invention to establish a power down mode by selecting a low frequency for the clock via the frequency dividing ratio setting part [53] in the circuit of Fujieda et al. to reduce wasteful power consumption since such configuration for the stated purpose has been a well known practice as evidenced by the teachings of Muraki et al. *(see Muraki et al., col. 1, lines 41-45).*

With respect to claim 15, the combined teaching of Fujieda et al. and Muraki et al., discloses that the frequency of the second clock signal is 2M when the frequency of the first clock signal is M *(since 53 selects the dividing ratio for divider (36,38), dividing ratio can be selected so that the first clock signal frequency (power down mode) is M and the second clock signal frequency is 2M (non-power down).*

Remarks

With respect to Applicant's argument regarding claim 14, on page 3, stating that Muraki makes some suggestions in very general term and even if Fujieda and Muraki are combined, they still do not teach the independent claim 14. The examiner respectfully disagrees.

Fujieda et al. discloses using the divider in his circuit to output the first clock signal or the second clock signal (divided clock signal) without explicitly expressing the purpose to lower power consumption. Muraki et al. discloses, in column 1, lines 41 to 45, that one of various

means for power down modes is to reduce the frequency of the clock and it is obviously understood by one skilled in the art that clock divider is one of the means to reduce frequency of the clock. Conclusively, the combined teachings of Fujieda et al. and Muraki et al. indeed disclose limitations claimed in independent claim 14.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER